RESEARCH STATEMENT

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Motivation:

My research focus is in the area of reliable, low power and high performance design of chip multiprocessors. With the ever shrinking feature size of today's complex VLSI Systems, there is a need for increased emphasis on newly developing research topics, such as leakage power, interconnect delay, noise, soft errors, power delivery and reliability. These problems, termed technology scaling challenges, need novel design approaches and solutions in many levels starting from circuit through CAD to architecture. The primary motivation behind my research is to explore micro-architectural techniques that mitigate the impact of process variations in devices.

Intended Research – Impact of Process Variations in Multi-Core Architectures:

Multi-core architectures, or chip multiprocessors (CMP), have become a common way of reducing chip complexity and power consumption while maintaining high performance. Challenges in multi-core processor design include meeting demands for performance, power, and reliability.

Cores are becoming sufficiently small with technology scaling. As technology continues scaling down beyond 90nm, inter-die and intra-die variations in process parameters (e.g., channel length, width, and threshold) can result in significant variations in the circuit characteristics. Due to process variations, the maximum clock frequencies and the power consumptions of these on-chip cores in a CMP deviate from their designed values randomly. As a result, it leads to asymmetry among the cores that were designed to be symmetric in performance causing core-to-core (C2C) variations. Both hardware and software techniques are needed to address the problems created by C2C asymmetry. The process variation results in timing instabilities and leakage power variation.

Process variation is an ever-increasing challenge in microprocessor design. As part of my MS thesis I would like to study the effects caused by process variation and will try to provide a solution on how to reduce the impact of these effects in chip multiprocessors.