DESIGN AND ANALYSIS OF LOW POWER 10-TRANSISTOR FULL ADDERS USING NOVEL X-NOR GATES

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Abstract
Full adders are important components in applications such as digital signal processors (DSP) architectures and micro-processors. In this paper, we propose a technique to build a total of 3 low power 10 transistor full adder using x-nor gates. We have done around 10 simulation runs of each adder for different frequencies, load capacitance and input patterns. Almost all the new adders consume less power in high frequencies. Out of 3 adders last two adders consume less power as compared to first one. The power consumption is compared against the Static Energy Recovery Full-adder (SERF). One drawback of new adders is the threshold-voltage loss of pass transistors.

Index Terms – Arithmetic circuit, full adder, low power, XNOR.

1. INTRODUCTION
Low power circuit design has emerged as a major technology driver due to growing markets in portable computing and communication systems. Low power technology strongly affects battery size and design, electronic packaging of ICs, heat dissipation and circuit reliability. Therefore, low-power and low-energy VLSI has become an important issue in today's consumer electronics. The adder is one of the most critical components of a processor, as it is used in the arithmetic logic unit (ALU), in the floating-point unit, and for address generation in case of cache or memory access. The full adder performance would affect the system as a whole. In this paper we have made a variety of full adders. In total we have found 3 new adders. All the new adders uses 10 transistors. So they take very less space. So in portable devices they are very useful. These low power adders apply circuit level techniques using various pass transistors. But these low power adders have the problem of threshold loss as compared to complementary static CMOS adders i.e. logic value 1 is not the value of Vdd and logic value 0 may not be the value of 0V. However, they are certainly useful in building up larger circuits such as multiple bit input adders and multipliers. In this paper we propose a schematic approach to design 3 10-transistor full adders. These new adders also have the problem of threshold loss, however these adders are useful in large circuits such as multipliers. We are using a novel set of XNOR gates for creating the new adders. We have done around 10 simulation for each circuit so that we can have a better look on the practical application of these new adders. Almost all the new adders show low power consumption in high frequencies. First adder we implemented is SERF. Two other adders that we implemented are 9A, 9B and 13A. All are implemented using 10 transistors but the 9A and 9B consume on average 10% less power as compared to SERF adder. The rest of the paper is organized as follows: In Section 2 we briefly describe the previous work in literature. In Section 3 we propose the new adders. In Section 4 we present the simulation methodology and simulation results. In Section 5, we draw the conclusions.

2. PREVIOUS WORK
Full adder adds 2 bits A and B with Cin. It gives two outputs SUM and COUT. The following equation shows the relation to calculate SUM and COUT.

\[ \text{SUM} = A \oplus B \oplus C \]  
\[ \text{SUM} = \overline{A \oplus B} \oplus C \]  
\[ \text{Cout} = (A \cdot \overline{(A \oplus B)}) + (\text{Cin} \cdot (A \oplus B)) \]
SERF adder implements (2) and (3) using only 10 transistors. Newly proposed adders also implement (2) and (3) using XNOR gates.

3. NEW DESIGN

(A) - Novel X-NOR Gates
We propose a new XNOR gate which is named Groundless XNOR, or G-XNOR, because there is no direct connection to the ground. We use the X-NOR gate which has 4 transistors. Figure 1(A) and 1(B) shows two such transistors.

![Fig. 1A, 1B](image)

(B) - Full Adder
We use three modules, shown in above figure, to implement the full adder based on 2 equations. Module-1 and module-2 are XNOR gates and module- COUT is a multiplexer. The sum is generated by cascading module-1 and module-2. The function COUT is implemented by module-1 and module-COUT.

![Fig.2 : Adder Modules](image)

4. EXPERIMENT DESCRIPTION AND RESULT

We have performed several simulation on SERF adder and newly proposed adders. The transistor have a channel length of 0.4 um and channel width for PMOS is 2um and for NMOS is 1.5um. Each circuit is simulated using same conditions.

The new adders will work smoothly within the frequency range 50KHZ to 50MHz. So for simulation purpose here we used 2 frequencies in that range ,i.e., 100KHz and 500KHz. Also 2 different load capacitances are used to load the circuit. Thus for each adder we had performed 4 simulations (2 frequencies *2 capacitances).

![Fig.3: Different Adders](image)

<table>
<thead>
<tr>
<th>Adder</th>
<th>Frequency</th>
<th>Load Capacitance</th>
<th>Power (nW)</th>
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</thead>
<tbody>
<tr>
<td>SERF</td>
<td>100kHz</td>
<td>0.02pF</td>
<td>30.21</td>
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<tr>
<td></td>
<td>500kHz</td>
<td>0.02pF</td>
<td>188.07</td>
</tr>
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<td></td>
<td>100kHz</td>
<td>0.3pF</td>
<td>32.29</td>
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<td>500kHz</td>
<td>0.3pF</td>
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<td>23.12</td>
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<td>500kHz</td>
<td>0.02pF</td>
<td>164.31</td>
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<td>0.3pF</td>
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<td>Adder9B</td>
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<td>0.3pF</td>
<td>15.70</td>
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<tr>
<td>Adder13</td>
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<td>0.02pF</td>
<td>6.941</td>
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<tr>
<td>A</td>
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<td>0.02pF</td>
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<td>0.3pF</td>
<td>10.97</td>
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<tr>
<td></td>
<td>500kHz</td>
<td>0.3pF</td>
<td>141.51</td>
</tr>
</tbody>
</table>

Table 1: Observations

After the simulations all the newly proposed full adders are found to have less power consumption than previous SERF adder. Adders 9B and 13A give better performance consistently, while 9B too give better results in majority of cases than SERF adder.

The performance of many larger circuits are strongly dependent on the performance of full adder circuits that have been used. The new 10 transistor adder circuits presented in this paper are useful in making these large systems, such as high performance multipliers with low power consumption. Due to 10 transistors, area required is also less.
5. CONCLUSION
In this paper we have presented systematic approach to construct full adders using only 10 transistor. In total we constructed 4 adders out of which 3 are new and one is SERF. Based on our simulations, we conclude that new adders consume around 10-20% less power as compared to previous 10 transistor SERF adder.

REFERENCES:

Simulation Diagrams:

Fig. A: SERF schematic

Fig. B: Adder 9A schematic
Fig. C: Adder 9B schematic

Fig. D: Adder 13A schematic
Fig. E: SERF Layout

Fig. F: Adder 9A layout
Fig. I: SERF Waveforms

Fig. J: Adder 9A waveform
Fig. K: Adder 9B waveform

Fig. L: Adder 13A waveform