Naman Govil

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Education

2011–2016(expected) **B.Tech and M.S by Research in Electronics and Communication Engg**, *IIIT Hyderabad, India*, *CGPA – 8.96/10*.

2011 **Senior Secondary**, *Bharatiya Vidya Bhavan's School*, Vadodara, *Percentage – 89%*.

2009 **Secondary**, *Bharatiya Vidya Bhavan's School*, Vadodara, *Percentage – 92%*.

Work Experience

March,2016–Present **Visiting Researcher**, Singapore University of Technology & Design (SUTD), Singapore.
Working on embedded security of Cyber-Physical Systems and large scale Industrial Control Systems such as PLCs.

May,2015–July,2015 **Research Intern**, Ecole Polytechnique de Montreal, Canada.
Awarded the Mitacs Globalink Scholarship and worked on designing low-cost space-grade systems based on FPGAs.

May,2014–August,2014 **Embedded Software Developer**, Google Summer of Code (GSoC), coreboot.
Involved in open-source hardware and software development. Worked on enhancing data access methods for ARM SoCs to ensure high performance and low SRAM consumption.

August,2013–April,2015 **Teaching Assistant (TA)**, IIIT Hyderabad.
Head TA for Embedded Hardware Design course and TA for Electronics Workshop II and Basic Electronic Circuits courses.

May,2013–July,2013 **Summer Intern**, Defence Research and Development Organisation (DRDO), Govt. of India.
Developed testing and debugging algorithms for various modules of the On Board Computer (OBC) of a Missile Interface Unit.

Publications

GMA: A High Speed Metaheuristic Algorithmic Approach to Hardware Software Partitioning for Low-cost SoCs, Naman Govil and Shubhajit Roy Chowdhury, *26th IEEE International Symposium on Rapid System Prototyping, October 2015, Amsterdam*.

High Performance and Low Cost Implementation of Fast Fourier Transform Algorithm based on Hardware Software Co-design, Naman Govil and Shubhajit Roy Chowdhury, *IEEE Tensymp, April 2014, Kuala Lumpur*.

Achievements

Academics Awarded the **Dean's Merit List** (top **5%** of the batch) for academic excellence for all four years of Bachelors.

Awarded the **ACM SIGBED ESWEEK 2015 Travel Grant** to attend and present a research paper at the IEEE RSP 2015, a part of ESWEEK 2015.

Research Awarded the **IIIT Research Award** (2014 and 2015) for outstanding undergraduate research.

IIT-JEE Secured All India Rank of 6352 **(98.81 percentile)** in IIT-JEE 2011 among 530000 candidates.

AIEEE Secured All India Rank of 5281 **(99.52 percentile)** in AIEEE 2011 among 1200000 candidates.

Technical skills

Languages	ARM-Assembly, C, C++ (STL), Verilog, VHDL.
Embedded Technologies	ATMEL-AVR, Arduino, ARM SoCs (Cubieboard), arm64 QEMU, Linux Kernel, USB, I2C, UART Protocols, Firmware Development.
Tools	Xilinx ISE, Vivado, Altera Quartus, Qsys, MATLAB, Multisim, ModelSim, Tanner-EDA, LT-SPICE, Cadence Virtuoso.
Others	Version Control - git.

Major Projects

Master's Project — **Algorithmic aspects of Hardware Software Partitioning**.
Guide: Dr. Shubhajit Roy Chowdhury, CVEST, IIIT Hyderabad
Worked on developing embedded system design techniques using Hardware Software Partitioning. Modeled Partitioning as a multi-objective optimization problem with the aim of minimizing area, power and run-time. Then, designed meta-heuristic algorithms to achieve pareto-optimal partitioning.

Summer 2015 — **Radiation Tolerant FPGA Architectures**.
Guide: Dr. Giovanni Beltrame, MIST Lab, Ecole Polytechnique de Montreal
Project aim was two-phased. First, worked on porting the open-source RISC processor (RISC-V), "Rocket Chip", to a non-ARM core based FPGA (Stratix-V). Next, implemented integration of the Xilinx SEM (Soft Error Mitigation) core into Rocket Chip design to perform fault insertion and scrubbing on Zynq FPGA.

August - November 2013 — **High Performance Implementation of Fast Fourier Transform Algorithm based on Hardware Software Co-design**.
Guide: Dr. Shubhajit Roy Chowdhury, CVEST, IIIT Hyderabad
Developed a high-performance and low cost implementation of the Fast Fourier Transform (FFT) algorithm using Hardware Software Co-design. Performance critical processes were run on an FPGA whereas less computationally-intensive components ran in software.

Other Projects

April - August 2015 — **Arm64 QEMU support for coreboot**, Open Source Development.
Guide: Marc Jones, coreboot
Initiated a port of coreboot for aarch64 emulation (QEMU). It involved scaling up bootblock and romstage stages to run in 64-bit. This project was the first of its kind to also bring in support for MacOS on coreboot for arm64 cross-compiling, multi-architecture gdb, etc. atop the conventional linux support.

January 2014 — **Sound Triangulation and Localization**.
Guide: Dr. Jayanthi Sivaswamy, CVIT, IIIT Hyderabad
Built a sound triangulation device based on signal processing on MATLAB, which tracks the speaker and remains directed towards him while he speaks. Once the speaker has completed, the device begins scanning the sample space for the next speaker and directs itself towards him.

December 2013 — **Mess"E"**.
Guide: Amy Canham, MIT Media Lab
Built an online food management system for university messes which enabled students to manage daily registrations and cancellations. It also coordinated left-over food distributions among nearby shelter homes.

Relevant Courses

- Computer Architecture
- Digital, ASIC and Embedded System Design
- Hardware Verification

Extra-Curricular Activities

- Founding Member and Coordinator (Till April 2015) at IIIT Hyderabad Electronics Club.
- Captain of Sports Council at IIIT-H (2014) and member of University Soccer team.